WHAT IS CLAIMED IS:

1. A driving circuit for a flat display device, applying a first voltage to a first electrode of a capacitive load serving as a display element and applying a second voltage having a phase opposite to the first voltage to the first electrode of the capacitive load, so as to make the display element emit light, comprising:

a power supply circuit for generating the first voltage and the second voltage to be applied to the capacitive load using an externally supplied power supply; and

a ramp waveform generation circuit connected between a first signal line supplying the first voltage and a second signal line supplying the second voltage generated by said power supply circuit so as to generate a ramp waveform to be applied to the capacitive load.

2. The device according to claim 1, wherein said ramp waveform generation circuit comprises a switching circuit and a resistor, connected to the ground.

3. The device according to claim 2, wherein said ramp waveform generation circuit further comprises a conversion circuit for converting a supplied control signal for said switching circuit to a drive level which allows said switching circuit to operate.

4. The device according to claim 2, wherein said ramp waveform generation circuit comprises a potential adjusting circuit for adjusting a final potential of the output ramp waveform.

5. The device according to claim 2, wherein said ramp waveform generation circuit comprises a ramp adjusting circuit for adjusting a ramp of the output ramp waveform.

6. The device according to claim 5, wherein said ramp adjusting circuit comprises a resistor inserted into a gate-charge loop.

7. The device according to claim 1, wherein the ramp waveform to be applied to the capacitive load changes from a positive potential to a negative potential.

8. The device according to claim 1, wherein the flat display device is an AC-driven plasma display device.

9. A driving circuit for a flat display device, applying a first voltage to a first electrode of a capacitive load serving as a display element and applying a second voltage having a phase opposite to the first voltage to the first electrode of the capacitive load, so as to make the display element emit light, comprising:

first and second switching circuits connected in series between the ground and an externally supplied power supply;

a capacitor having one terminal connected to a interconnection node between said first and second switching circuits;

a third switching circuit connected between the ground and the other terminal of said capacitor; and

a fourth switching circuit and a first resistor, connected in series between the ground and the interconnection node between said first and second switching circuits.

10. The device according to claim 9, further comprising a Zener diode having one terminal connected to the interconnection node between said first and second switching circuits, and

said fourth switching circuit and said first resistor are connected in series between the ground and the other terminal of said Zener diode.

11. The device according to claim 9, further comprising a driver circuit for converting a supplied control signal to a drive level which allows said fourth switching circuit to operate and outputting the control signal to said fourth switching circuit.

12. The device according to claim 11, further comprising a second resistor connected in series between an output terminal of said driver circuit and a control signal input terminal of said fourth switching circuit.

13. The device according to claim 9, wherein the flat display device is an AC-driven plasma display device.

14. The device according to claim 1, wherein said ramp waveform changes in its voltage with time elapsing at a constant rate in relation to the time elapse.

15. The device according to claim 1, wherein said ramp waveform changes in its voltage with time elapsing at a rate that varies with time elapsing.

16. The device according to claim 1, further comprising a capacitor connected between said first and second signal lines,

wherein said ramp waveform generation circuit is connected to an interconnection point between said first signal line and said capacitor.